AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently Amended) A method for manufacturing a semiconductor device having the step of forming a wiring by a damascene method, comprising the steps of:

forming an etching stopper film and an interlayer insulating film in sequence over a conductive layer;

forming a silicon carbide film, a silicon nitride film, or a silicon oxynitride film as a first hard mask over the interlayer insulating film;

forming a silicon oxide film as a second hard mask over the first hard mask;

forming a silicon carbide film or a silicon nitride film as a third hard mask over the second hard mask;

forming a silicon oxide film as a fourth hard mask over the third hard mask;

forming a pattern over the fourth hard mask;

etching the fourth hard mask by using the pattern;

etching the third hard mask [[with]] by using the fourth hard mask;

etching the second hard mask [[with]] by using the third hard mask;

etching the first hard mask [[with]] by using the third hard mask;

forming an opening which reaches the etching stopper film in the interlayer insulating film by etching the interlayer insulating film [[with]] by using the third hard mask;

etching a portion of the etching stopper film which is exposed from the opening formed in the interlayer ~~dielectric~~ insulating film;

and embedding a wiring material in the opening;

wherein a thickness of the third hard mask is more than twice that of the first hard mask.

2. (Original) The method for manufacturing the semiconductor device according to claim 1, wherein a low dielectric constant insulating film is used as the interlayer insulating film.

3. (Withdrawn) The method for manufacturing the semiconductor device according to claim 1, wherein an inorganic insulating film is used as the interlayer insulating film.

4. (Withdrawn) The method for manufacturing the semiconductor device according to claim 1, wherein a porous insulating film is used as the interlayer insulating film.

5. (Withdrawn) The method for manufacturing the semiconductor device according to claim 1, wherein a porous silica film is used as the interlayer insulating film.

6. (Original) The method for manufacturing the semiconductor device according to claim 1, wherein the etching stopper film is a silicon carbide film or a silicon nitride film.

7. (Cancelled)

8. (Original) The method for manufacturing the semiconductor device according to

claim 1, wherein said step of etching the etching stopper film comprises the step of removing the third hard mask.

9. (Currently Amended) The method for manufacturing the semiconductor device according to claim 1, wherein said step of etching the second hard mask [[with]] by using the third hard mask comprises the step of removing the fourth hard mask.

10. (Withdrawn) The method for manufacturing the semiconductor device according to claim 1, wherein said step of forming the pattern over the fourth hard mask comprises the steps of:

forming a first pattern over the fourth hard mask with a first resist mask;

removing the first resist mask;

forming a resin film over an entire surface;

forming a pattern over the resin film with a second resist mask;

forming a second pattern over the fourth hard mask with the resin film as a mask; and

removing the resin film.

11. (Withdrawn) The method for manufacturing the semiconductor device according to claim 10, wherein the first pattern is a wiring trench pattern and the second pattern is a via hole pattern.

12. (Withdrawn) The method for manufacturing the semiconductor device according to claim 10 further comprising, after said step of forming the second pattern over the fourth hard mask, the step of etching the third and second hard masks with the resin film.

13. (Withdrawn) The method for manufacturing the semiconductor device according to claim 11 further comprising, after said step of forming the second pattern over the fourth hard mask, the step of etching the third and second hard masks with the resin film.

14. (Withdrawn) The method for manufacturing the semiconductor device according to claim 12, wherein said step of etching the third hard mask with the fourth hard mask comprises the step of etching the first hard mask.

15. (Withdrawn) The method for manufacturing the semiconductor device according to claim 13, wherein said step of etching the third hard mask with the fourth hard mask comprises the step of etching the first hard mask.

16. (Withdrawn) The method for manufacturing the semiconductor device according to claim 14, wherein said step of etching the second hard mask with the third hard mask comprises the step of forming a hole which is shallower than the thickness of the interlayer insulating film, in the interlayer insulating film.

17. (Withdrawn) The method for manufacturing the semiconductor device according to claim 15, wherein said step of etching the second hard mask with the third hard mask comprises the step of forming a hole which is shallower than the thickness of the interlayer insulating film, in the interlayer insulating film.

18. (Withdrawn) The method for manufacturing the semiconductor device according to claim 10, wherein the opening includes a wiring trench portion formed based over the first pattern and a via hole portion formed over the second pattern.

19. (Withdrawn) The method for manufacturing the semiconductor device according to claim 11, wherein the opening includes a wiring trench portion formed based over the first pattern and a via hole portion formed over the second pattern.

20. (New) The method for manufacturing the semiconductor device according to claim 1, wherein said etching stopper film and said interlayer insulating film are formed in sequence in contact with said conductive layer; and

said first hard mask is formed in contact with the interlayer insulating film.

21. (New) A method for manufacturing a semiconductor device having the step of forming a wiring by a damascene method, comprising the steps of:

forming an etching stopper film and an interlayer insulating film in sequence in contact with a conductive layer;

forming a silicon carbide film, a silicon nitride film, or a silicon oxynitride film as a first hard mask in contact with the interlayer insulating film;

forming a silicon oxide film as a second hard mask in contact with the first hard mask;

forming a silicon carbide film or a silicon nitride film as a third hard mask in contact with the second hard mask;

forming a silicon oxide film as a fourth hard mask in contact with the third hard mask;

forming a pattern over the fourth hard mask;

etching the fourth hard mask by using the pattern;

etching the third hard mask by using the fourth hard mask;

etching the second hard mask by using the third hard mask;

etching the first hard mask by using the third hard mask;

forming an opening which reaches the etching stopper film in the interlayer insulating film by etching the interlayer insulating film, the interlayer insulating film is etched by using the third hard mask;

etching a portion of the etching stopper film which is exposed from the opening formed in the interlayer insulating film;

and embedding a wiring material in the opening.